VHDL予約語一覧

abs	downto	linkage	process	then
access	else	literal	pure	to
after	elsif	loop	range	transport
alias	end	map	record	type
all	entity	mod	register	unaffected
and	exit	nand	reject	units
architecture	file	new	rem	until
array	for	next	report	use
assert	function	nor	return	variable
attribute	generate	not	rol	wait
begin	generic	null	ror	when
block	guarded	of	select	while
body	if	on	severity	with
buffer	impure	open	shared	xnor
bus	in	or	signal	xor
case	inertial	others	sla	
component	inout	out	sll	
configuration	is	package	sra	
constant	label	port	srl	
disconnect	library	postponed	subtype	